



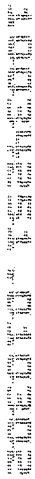
[illegible]

FIG. 3

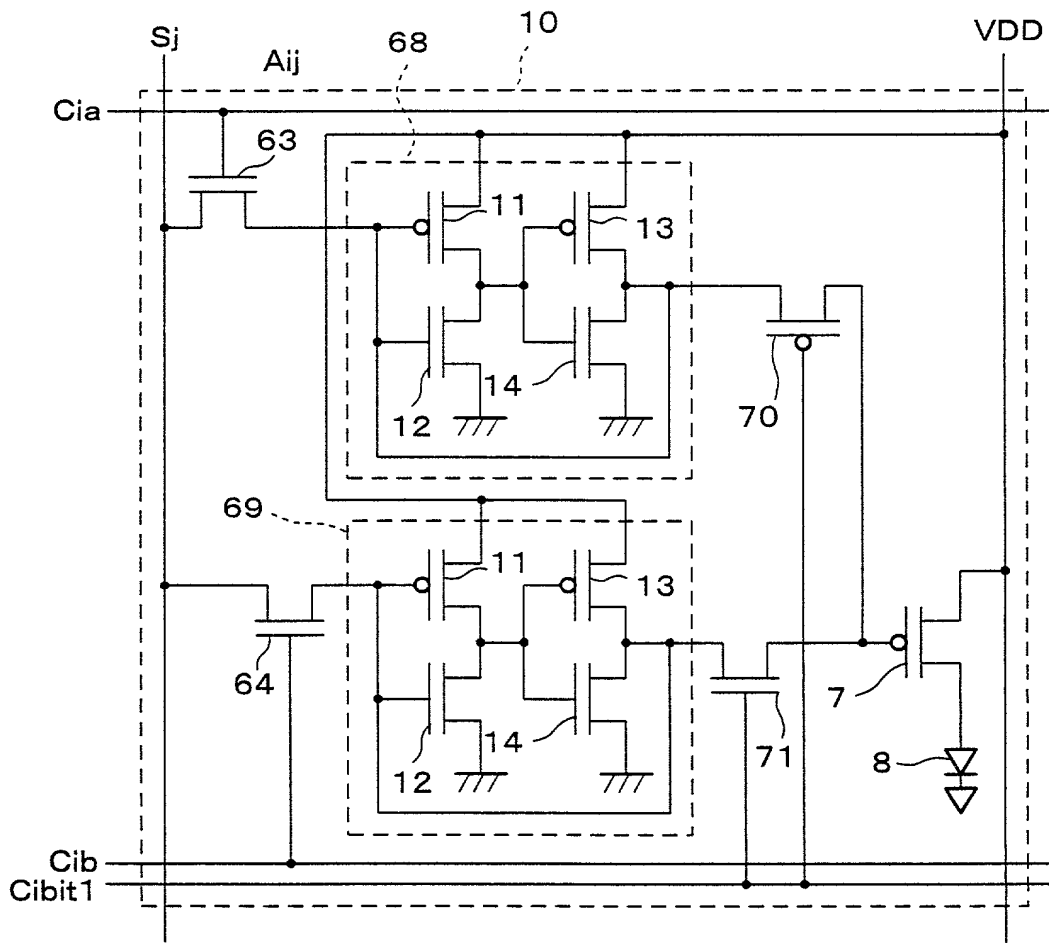


FIG. 4

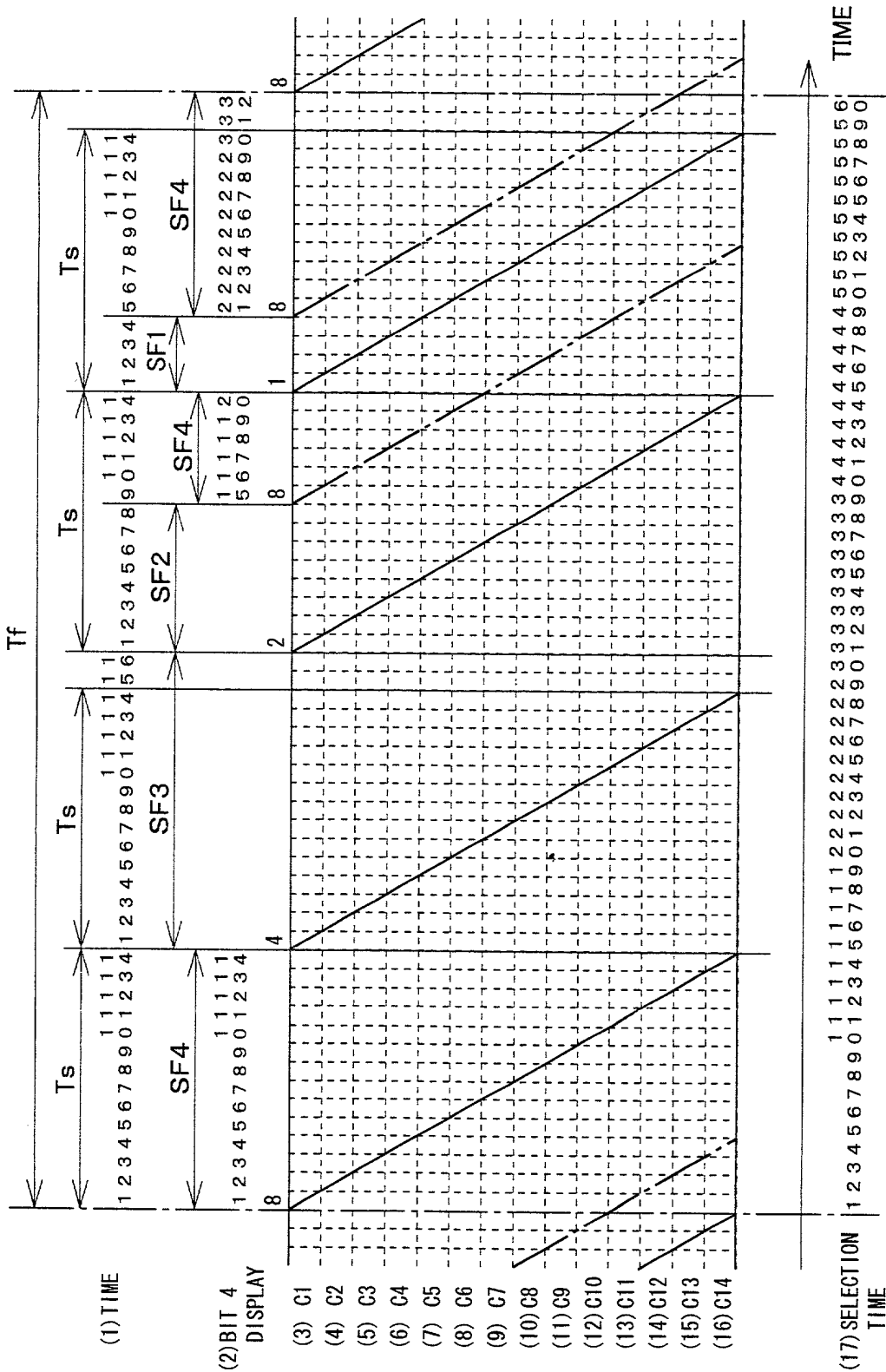


FIG. 5

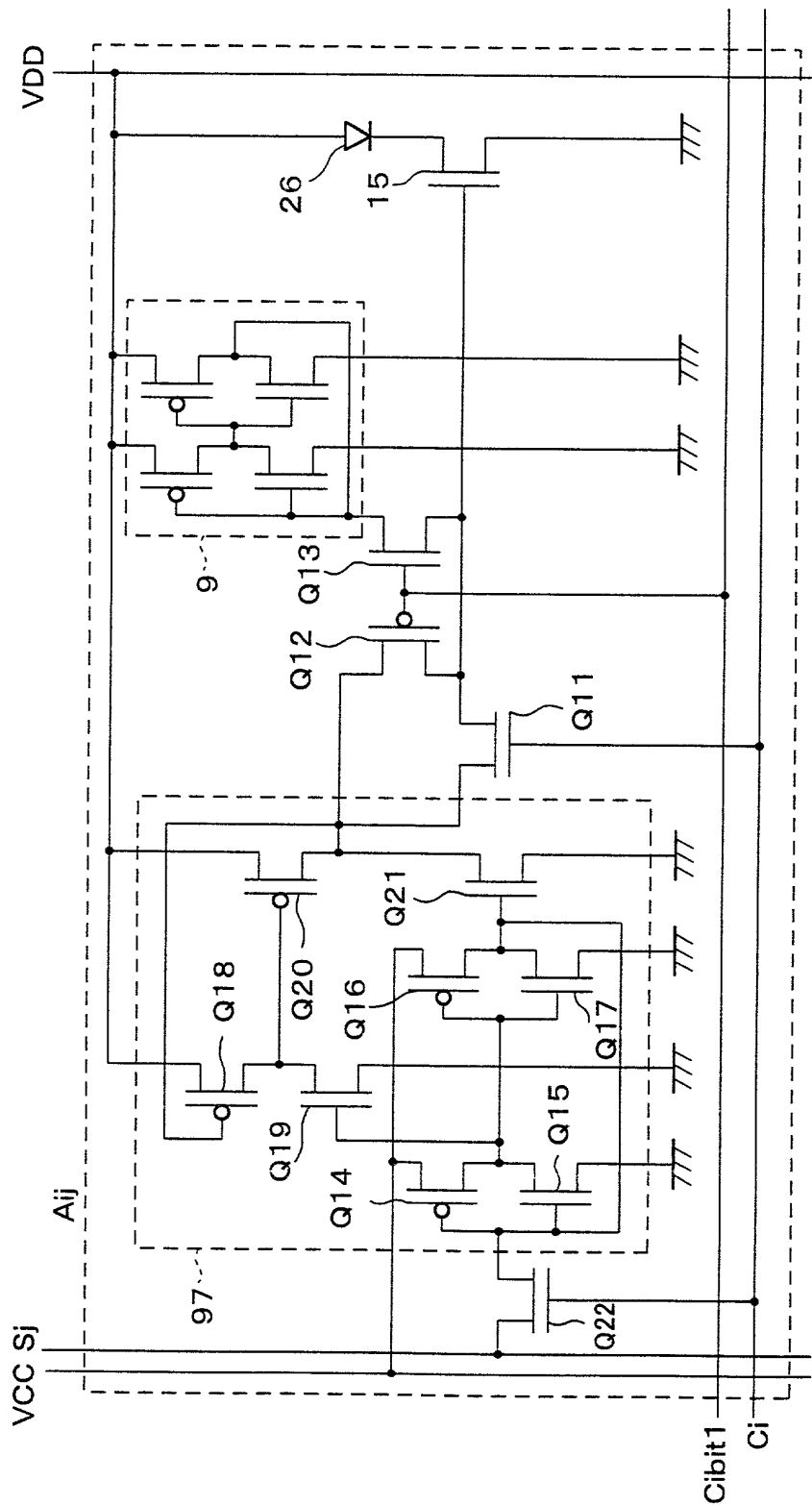


FIG. 6

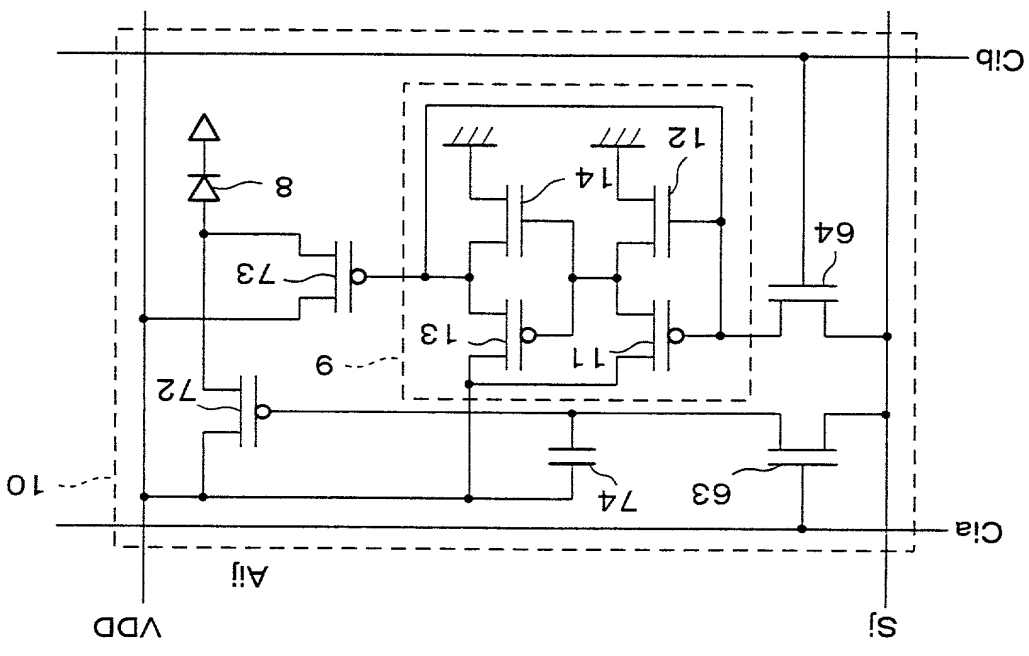


FIG. 6 is a circuit diagram of a multi-stage CMOS circuit, likely a differential signal path or a multi-bit data path. The circuit is bounded by a dashed rectangle. The input nodes are labeled S, A, and C, and the output nodes are labeled S, A, and C. The circuit includes several transistors: 11, 12, 13, and 14 are PMOS transistors, while 63, 64, 72, and 73 are NMOS transistors. A diode 8 is connected to the output node C. A resistor 10 is connected to the input node A. A capacitor 74 is connected to the input node S. The circuit is powered by VDD and ground. The output node S is connected to the input node S, the output node A is connected to the input node A, and the output node C is connected to the input node C. The circuit is a multi-stage CMOS circuit, likely a differential signal path or a multi-bit data path.

FIG. 7

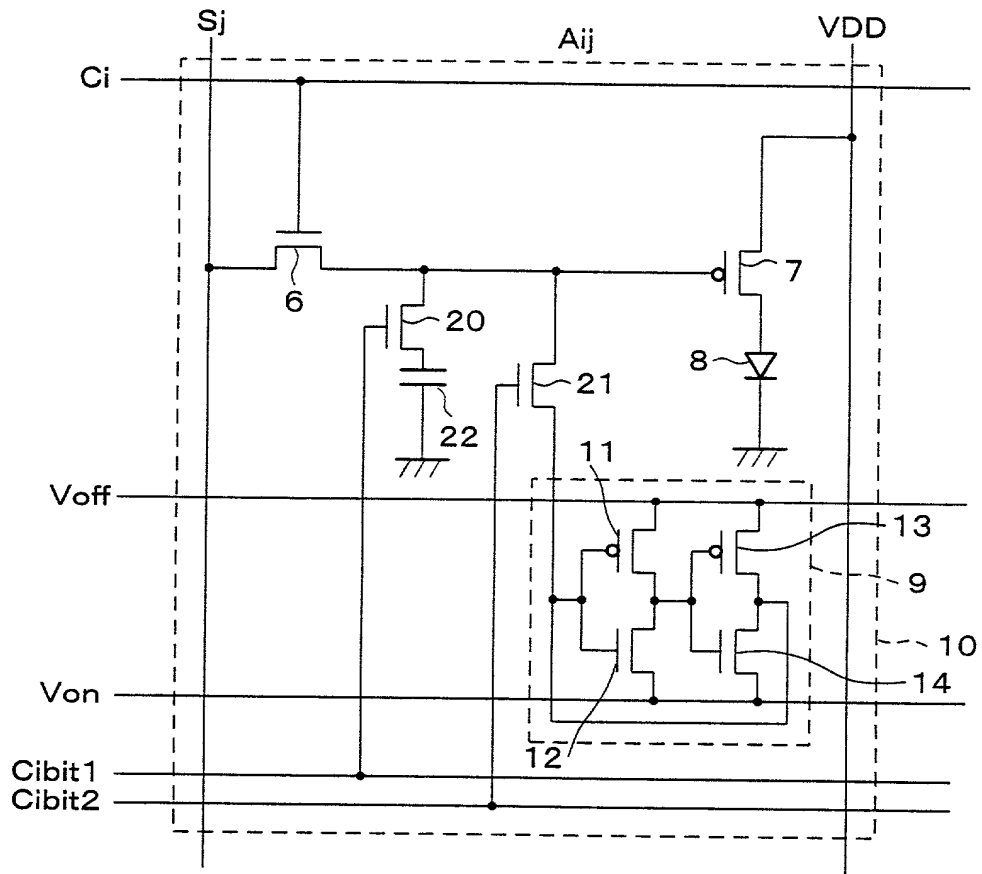


FIG. 8

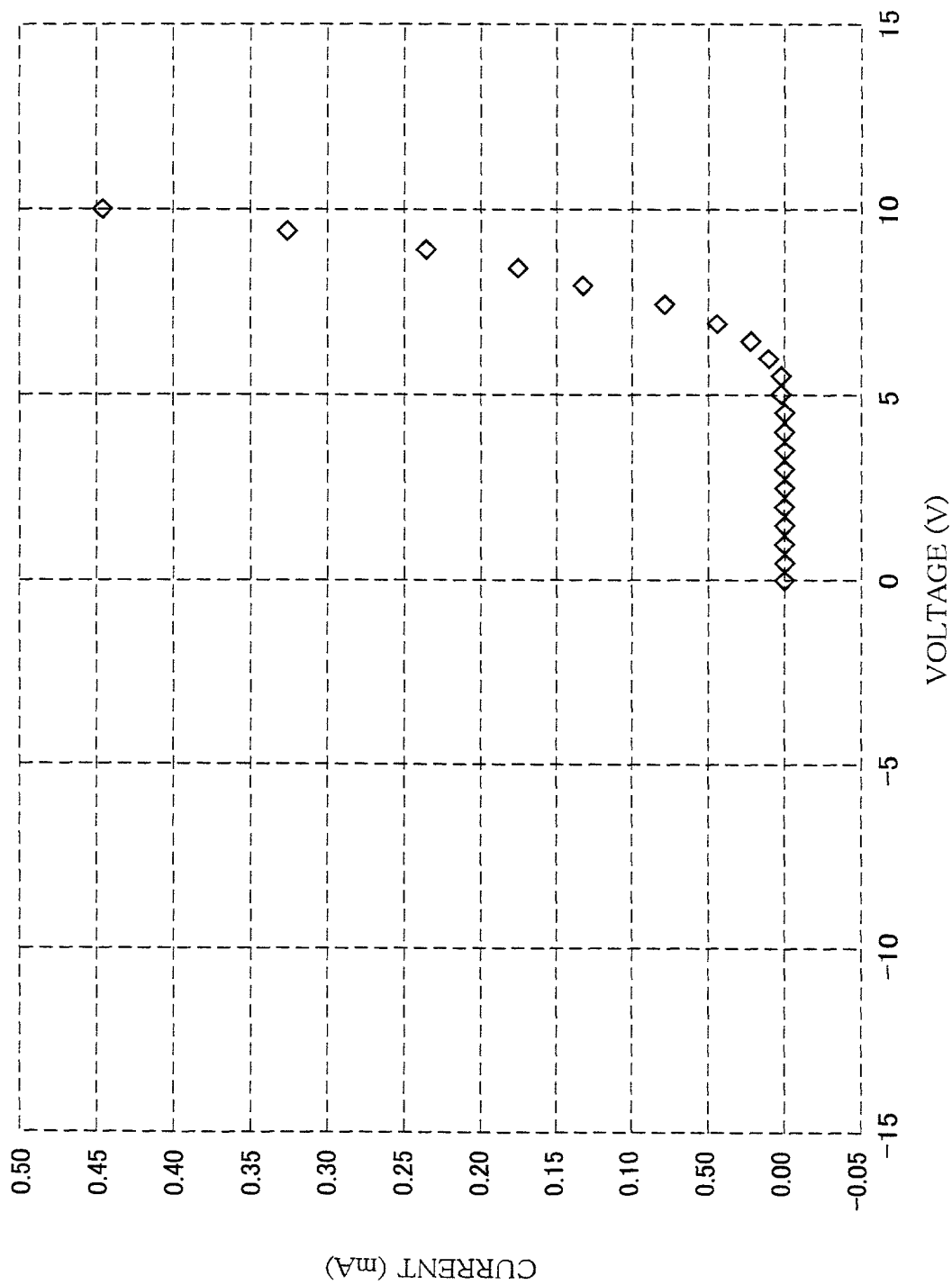


FIG. 9 (a)

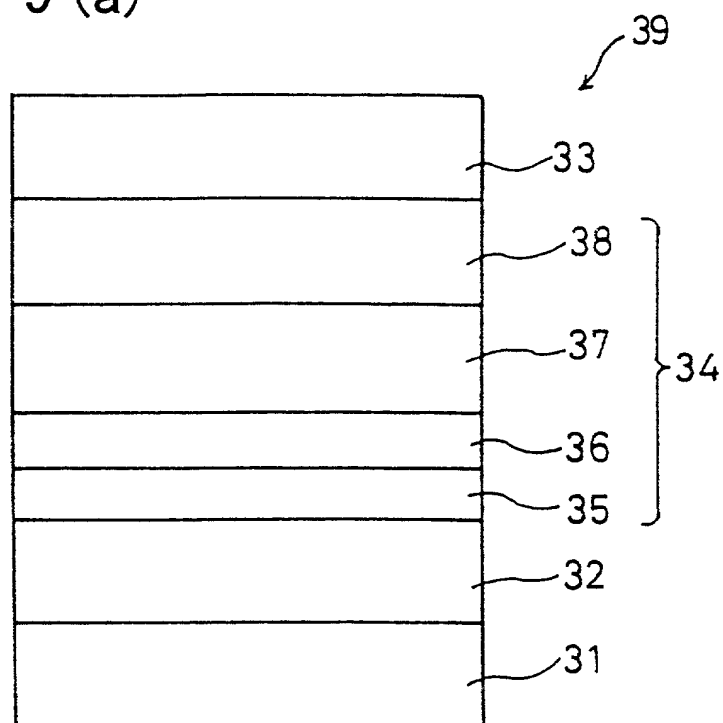


FIG. 9 (b)

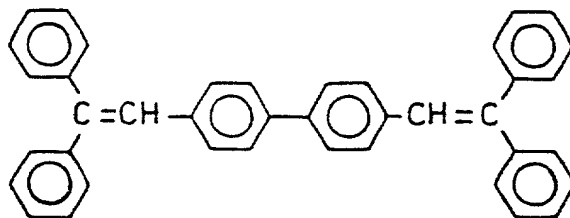


FIG. 10

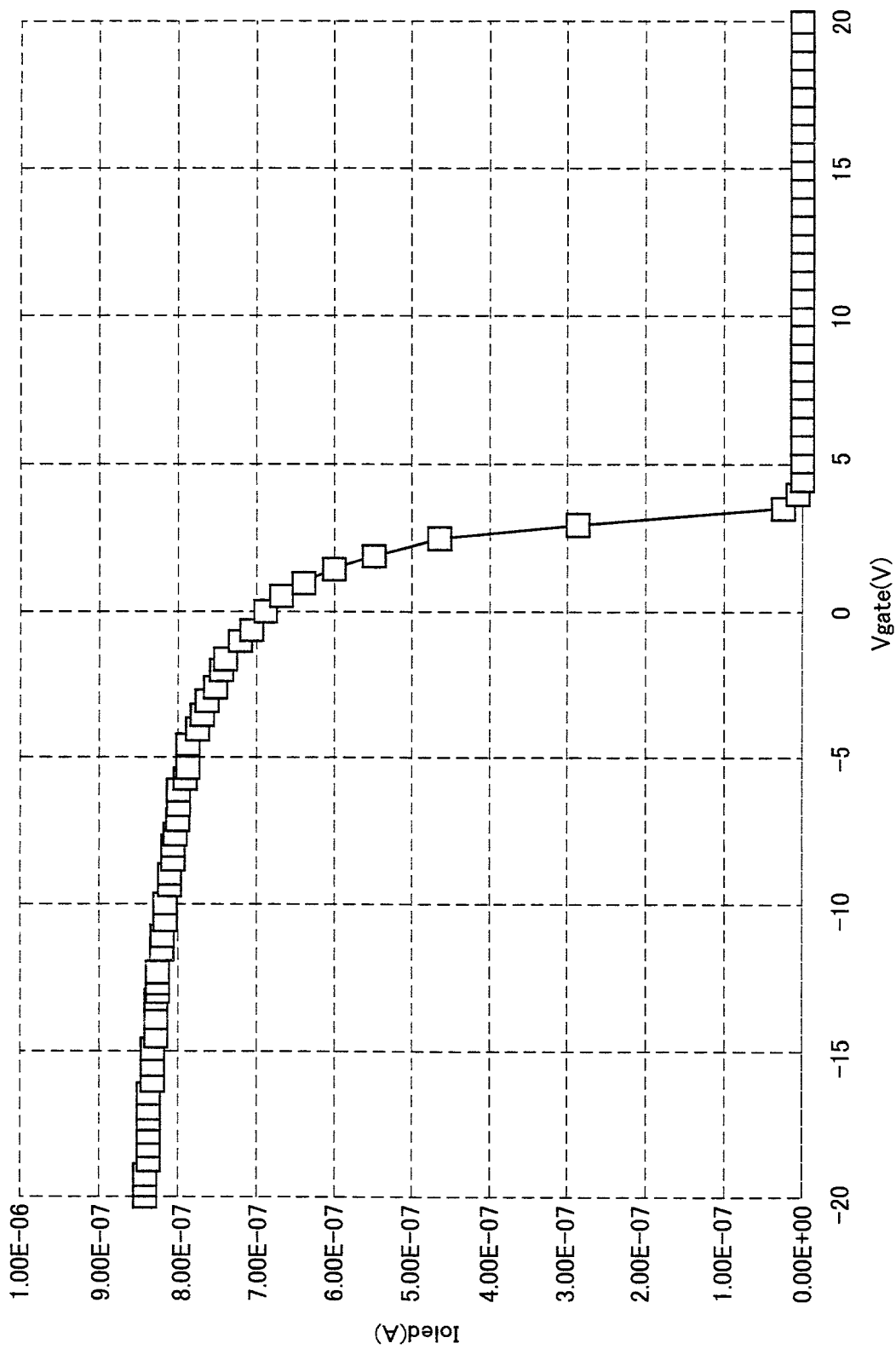


FIG. 11

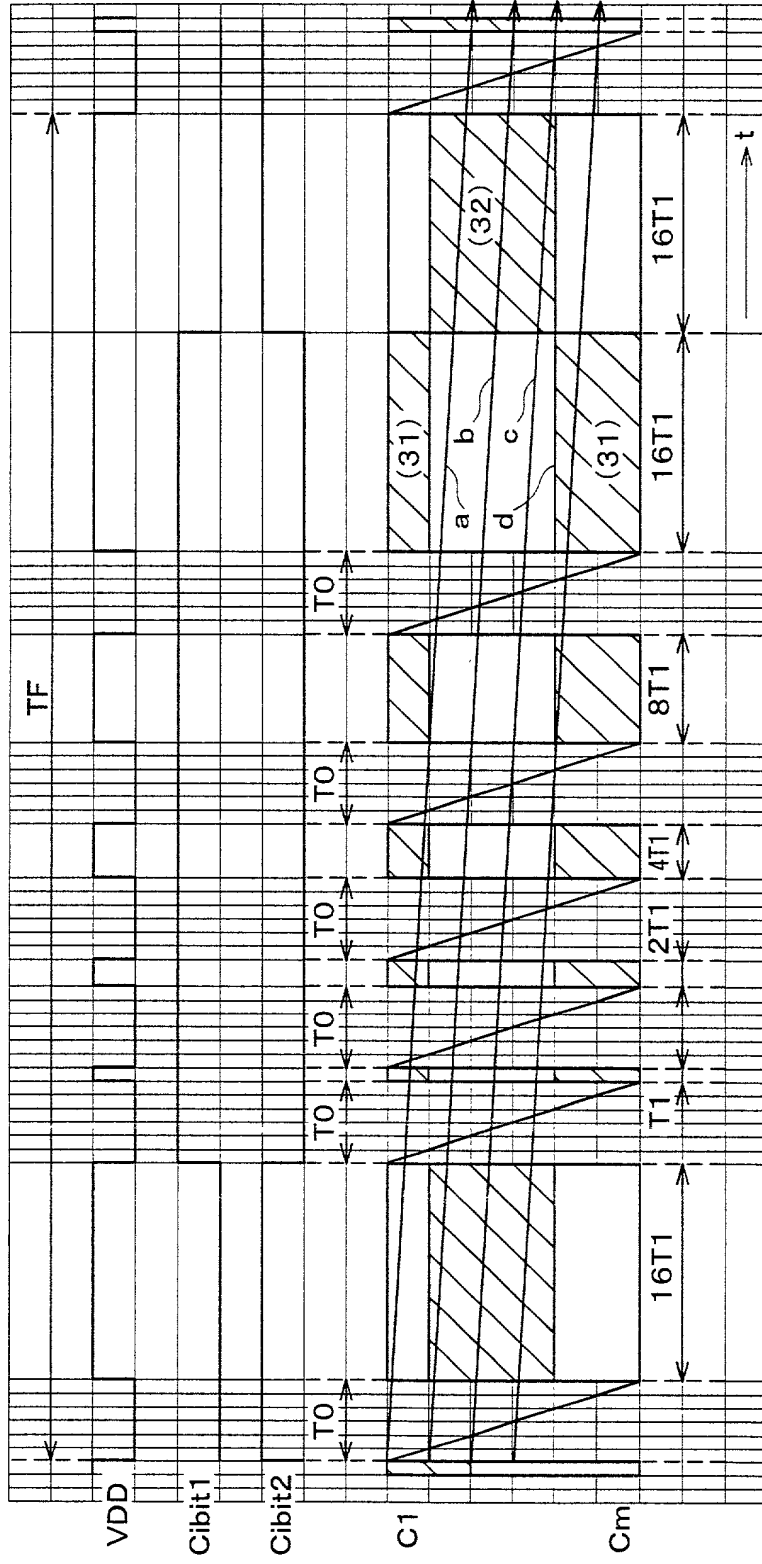


FIG. 12

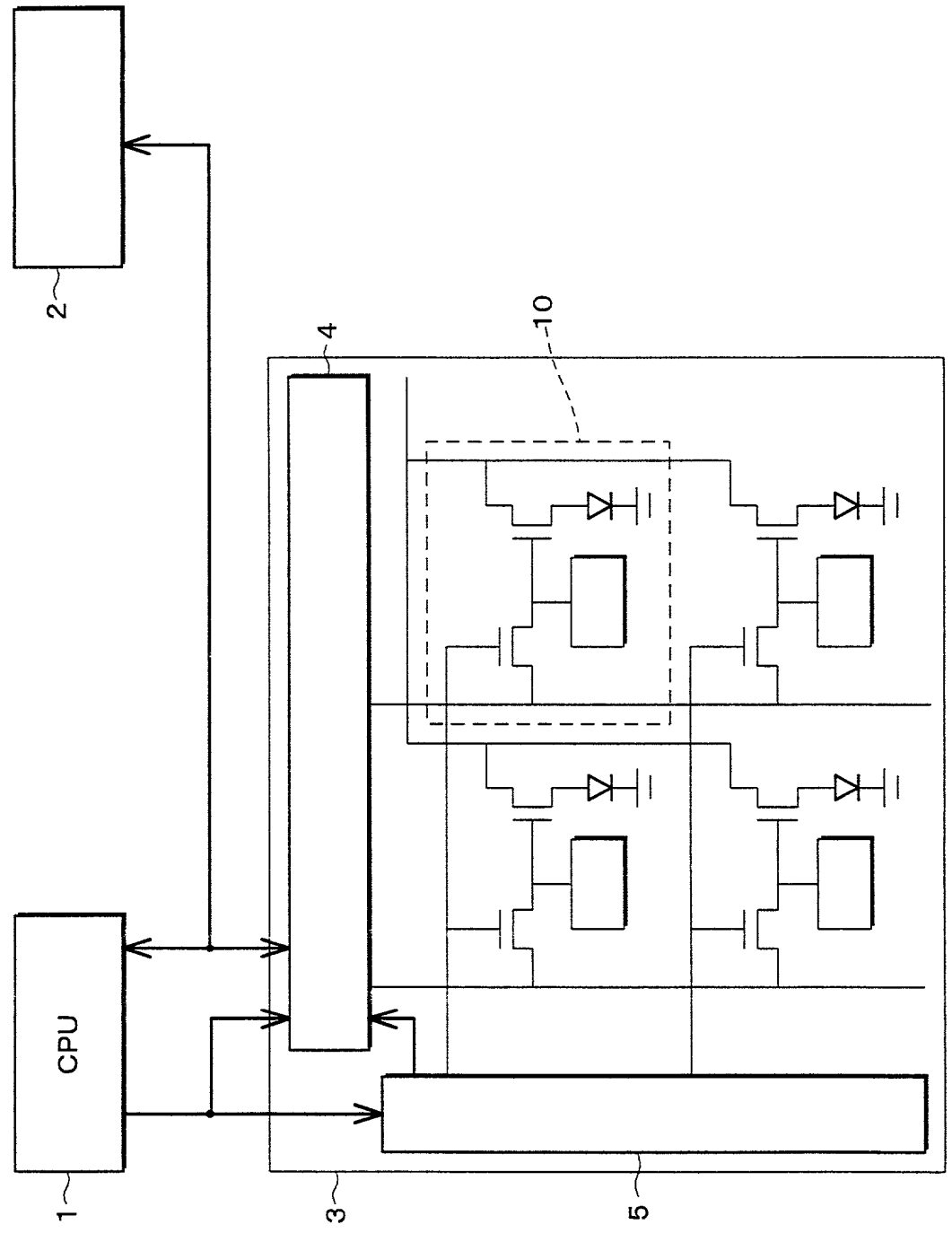
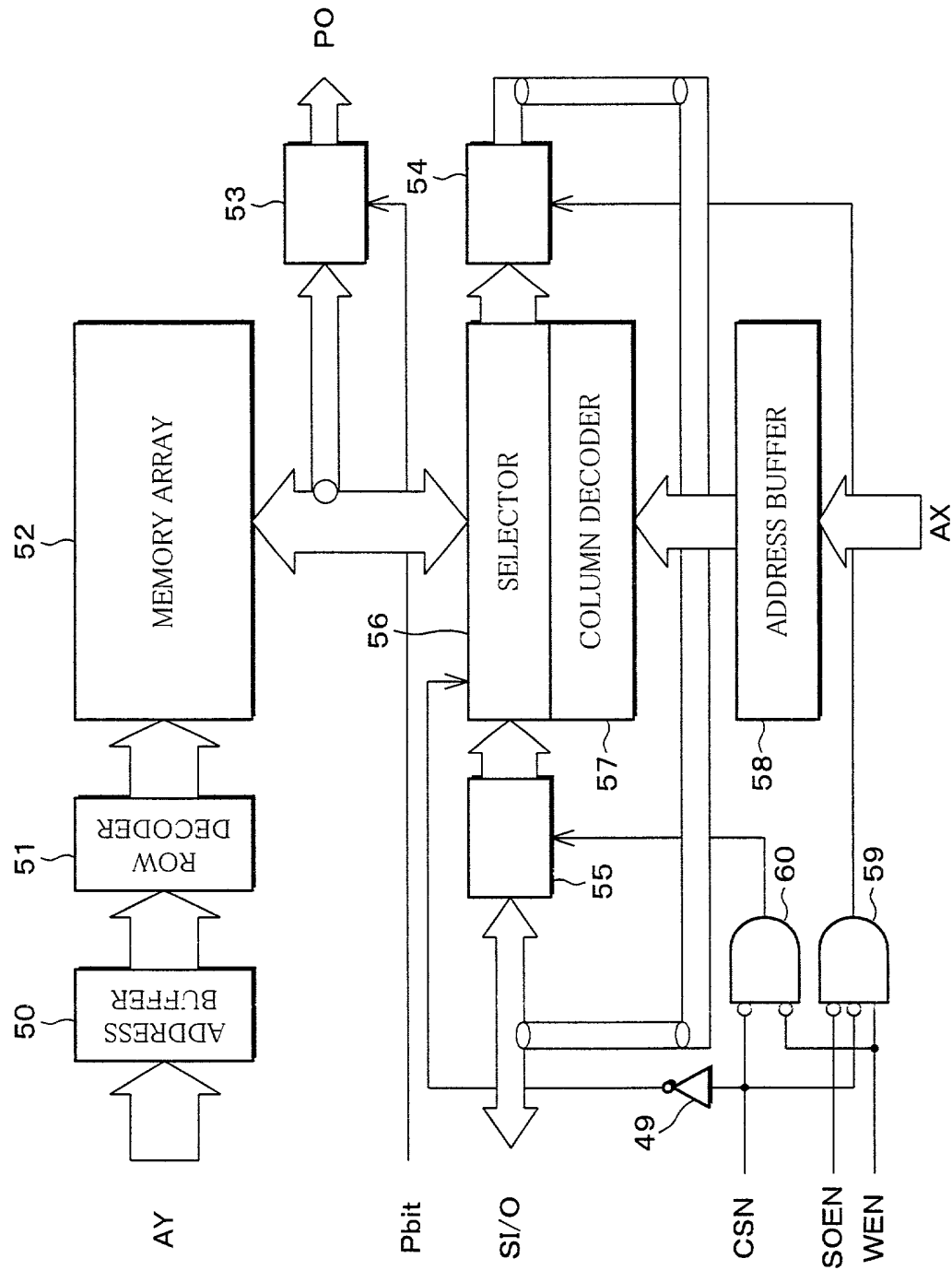


FIG. 13



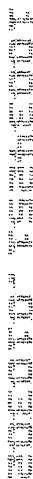
[illegible]

FIG. 15

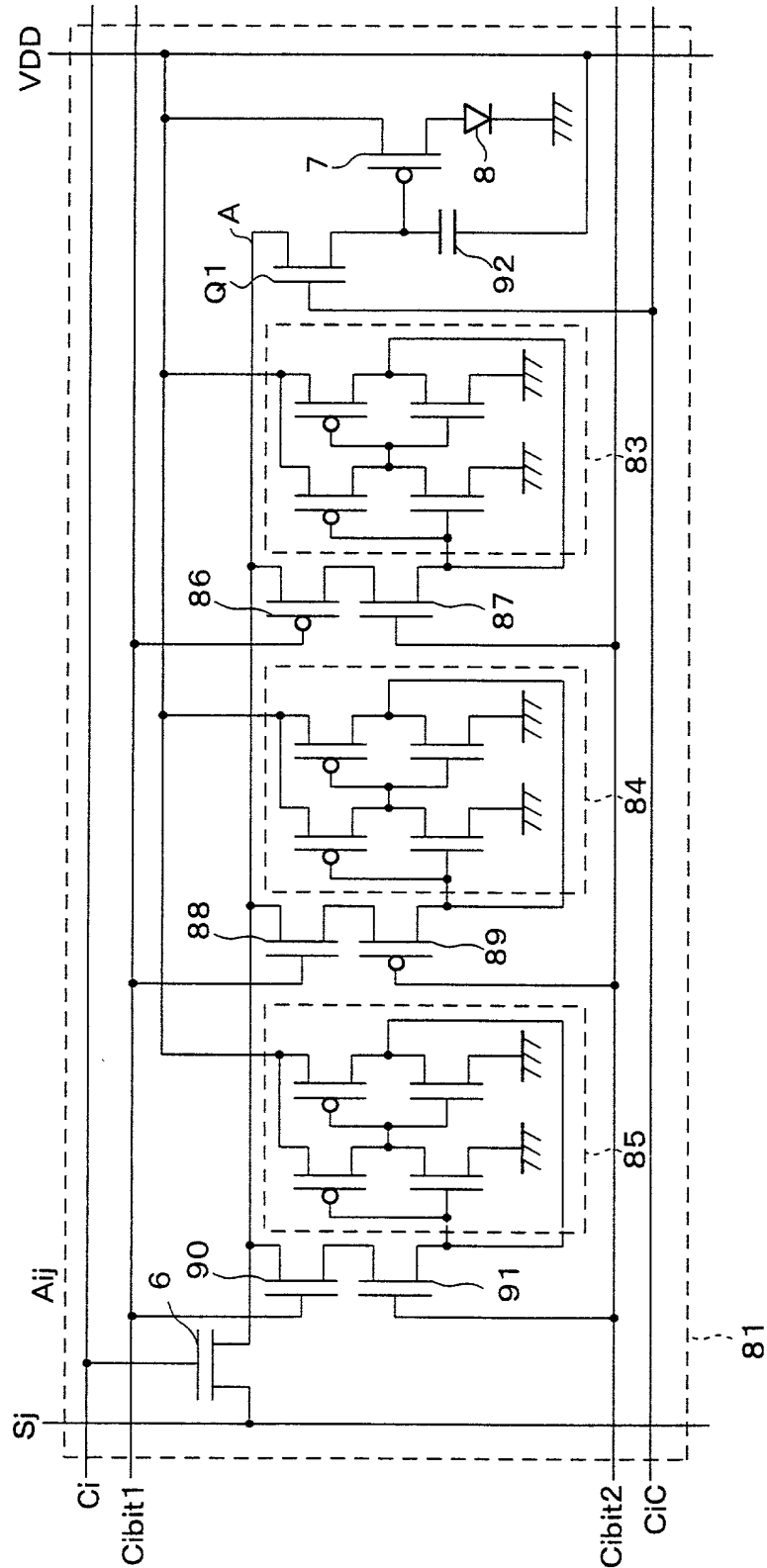
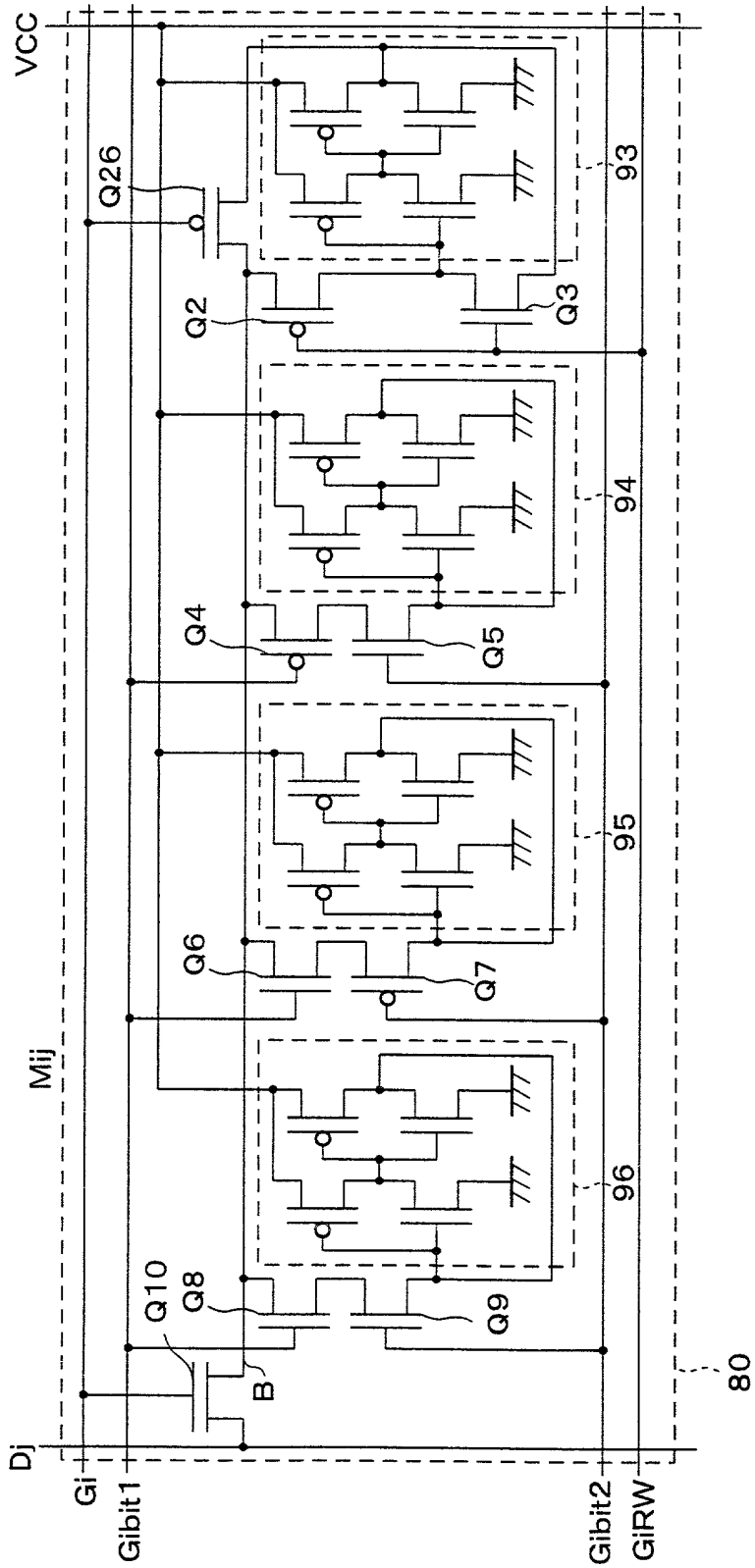


FIG. 16



[illegible]

FIG. 18

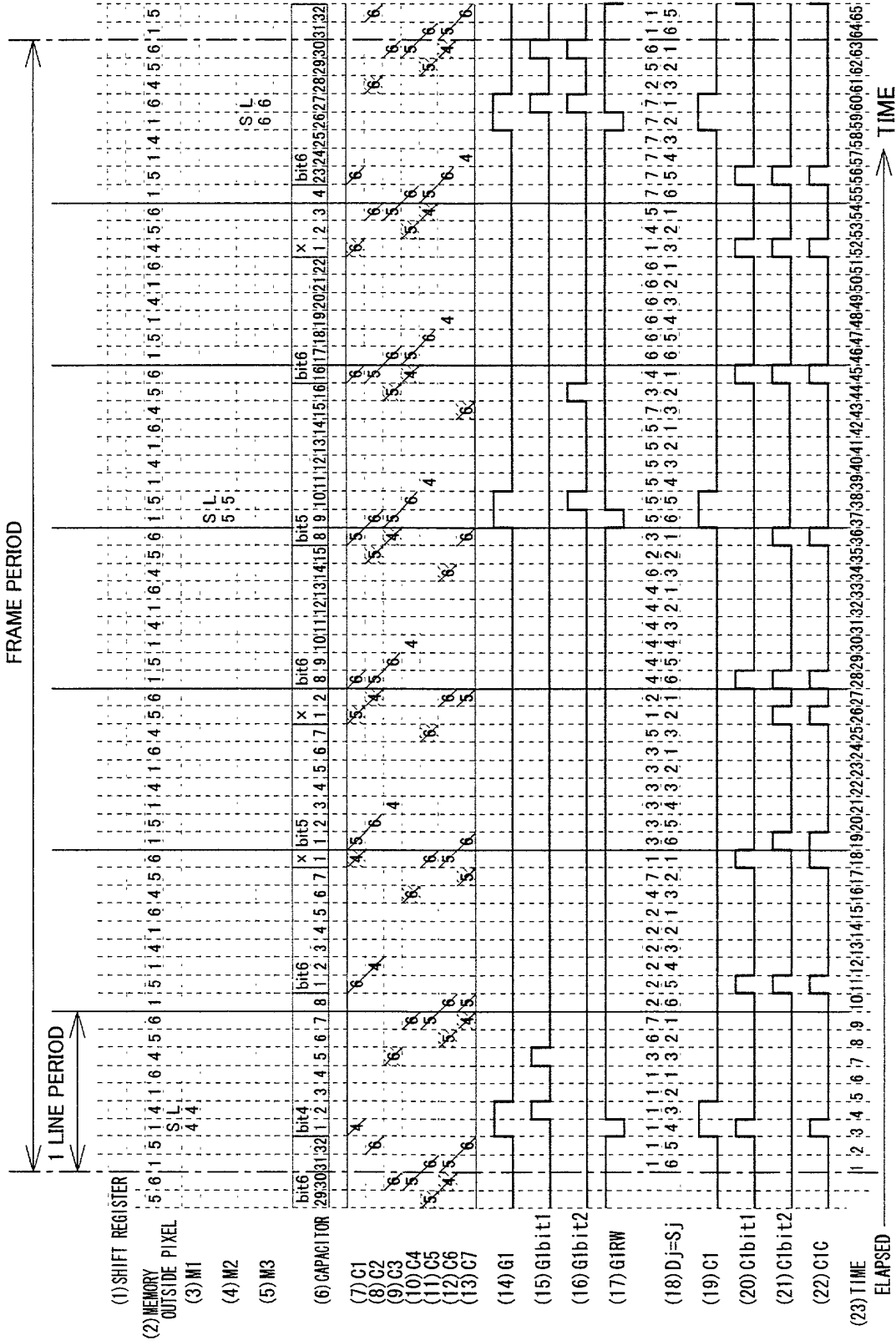


FIG. 19

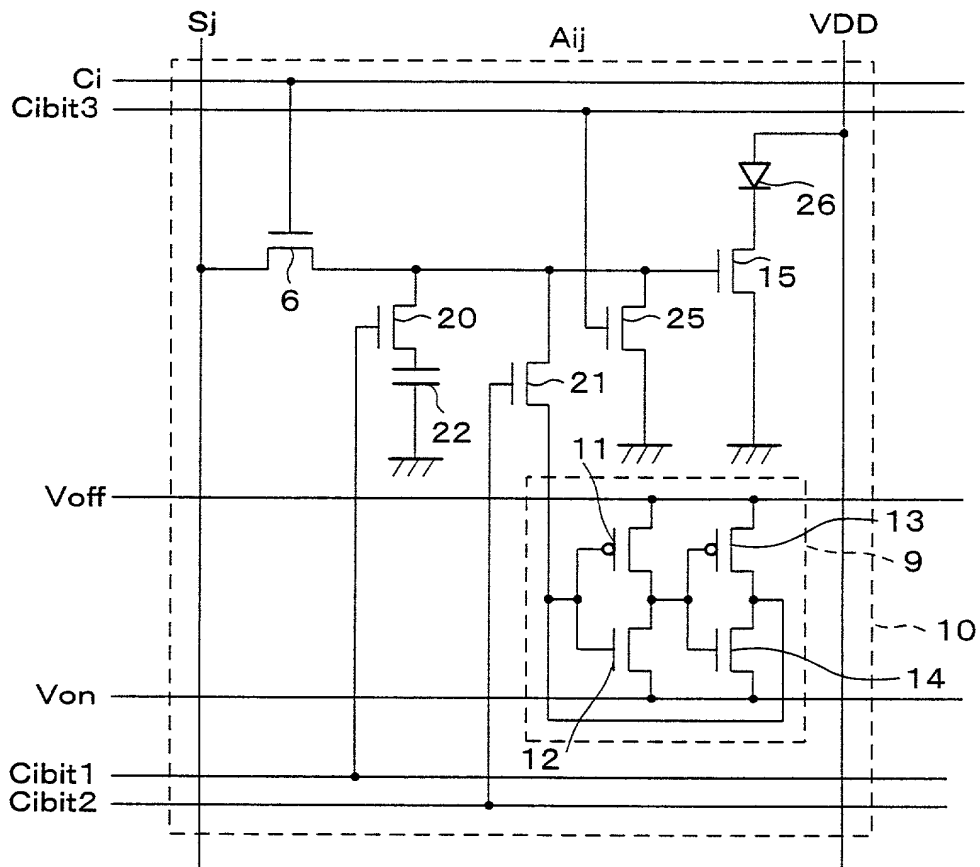


FIG. 20

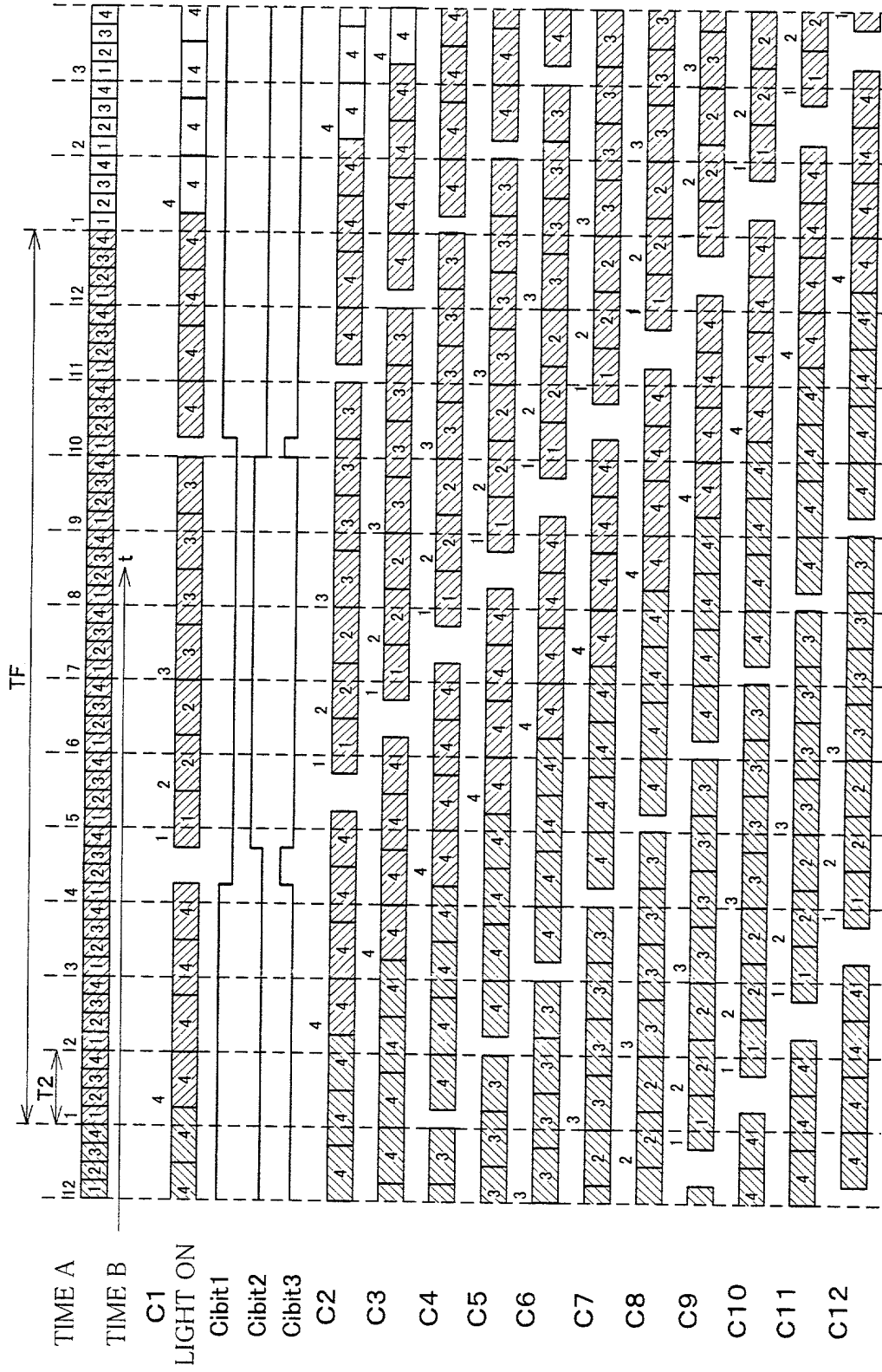


FIG. 21

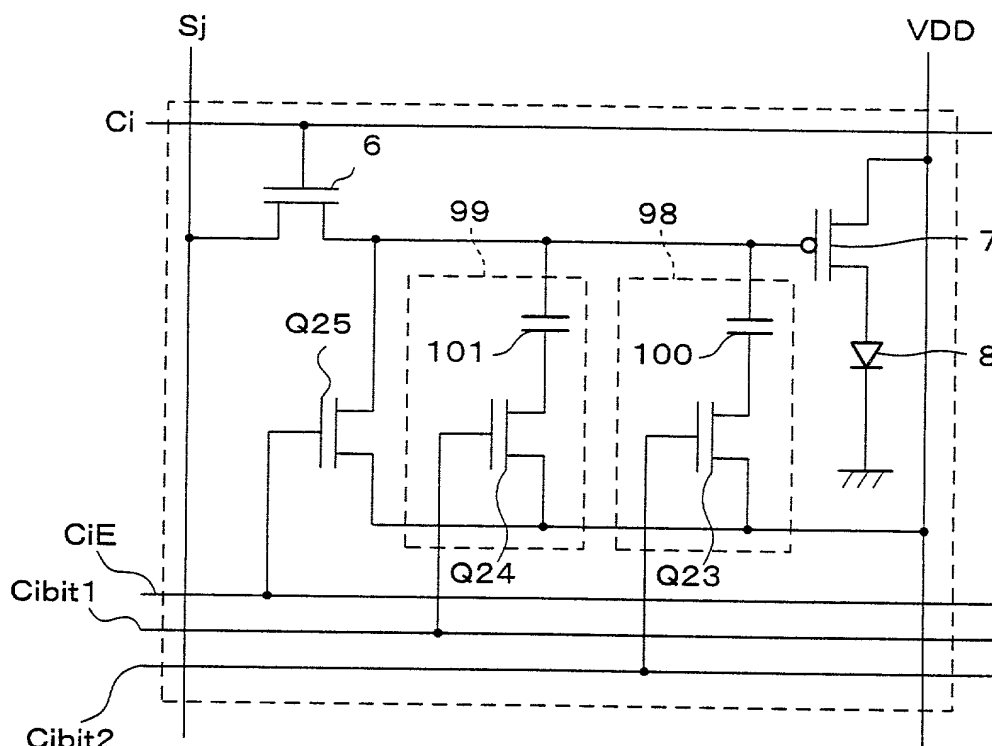


FIG. 22

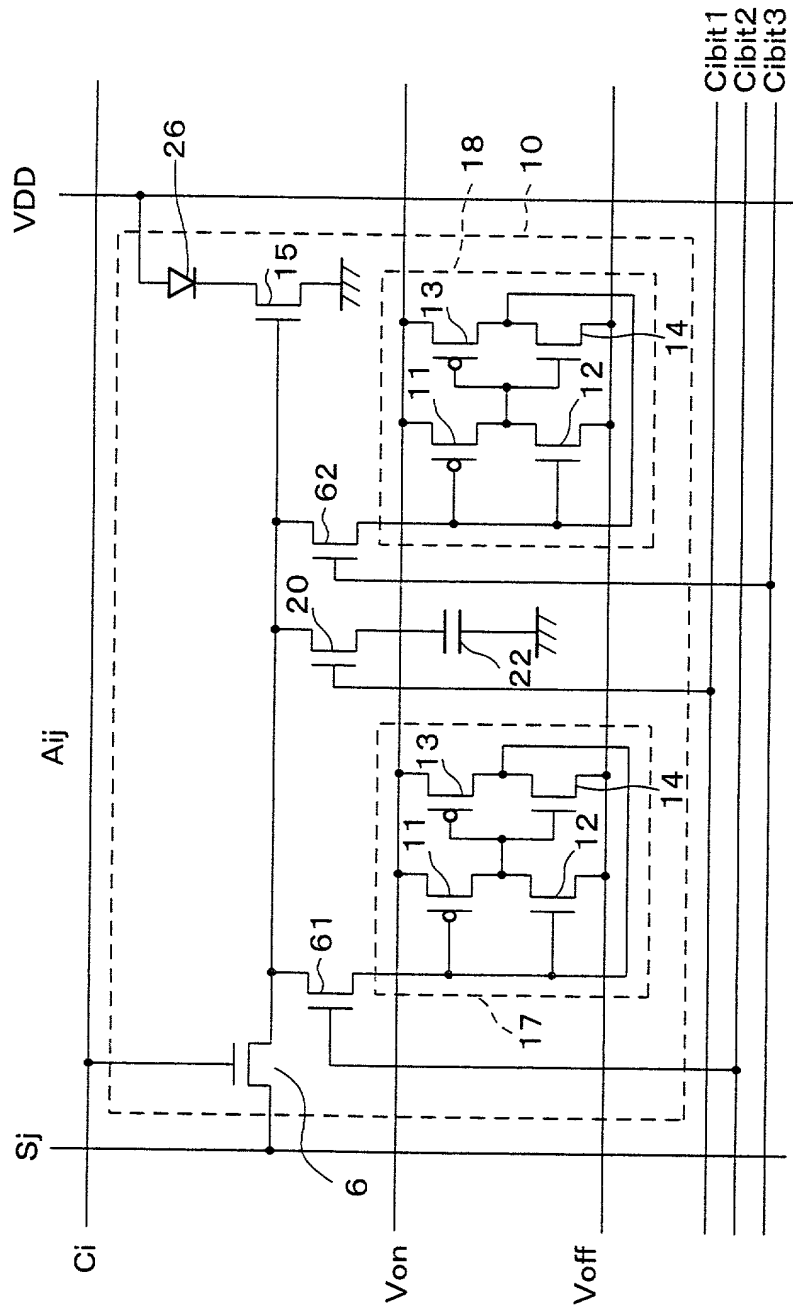


FIG. 23

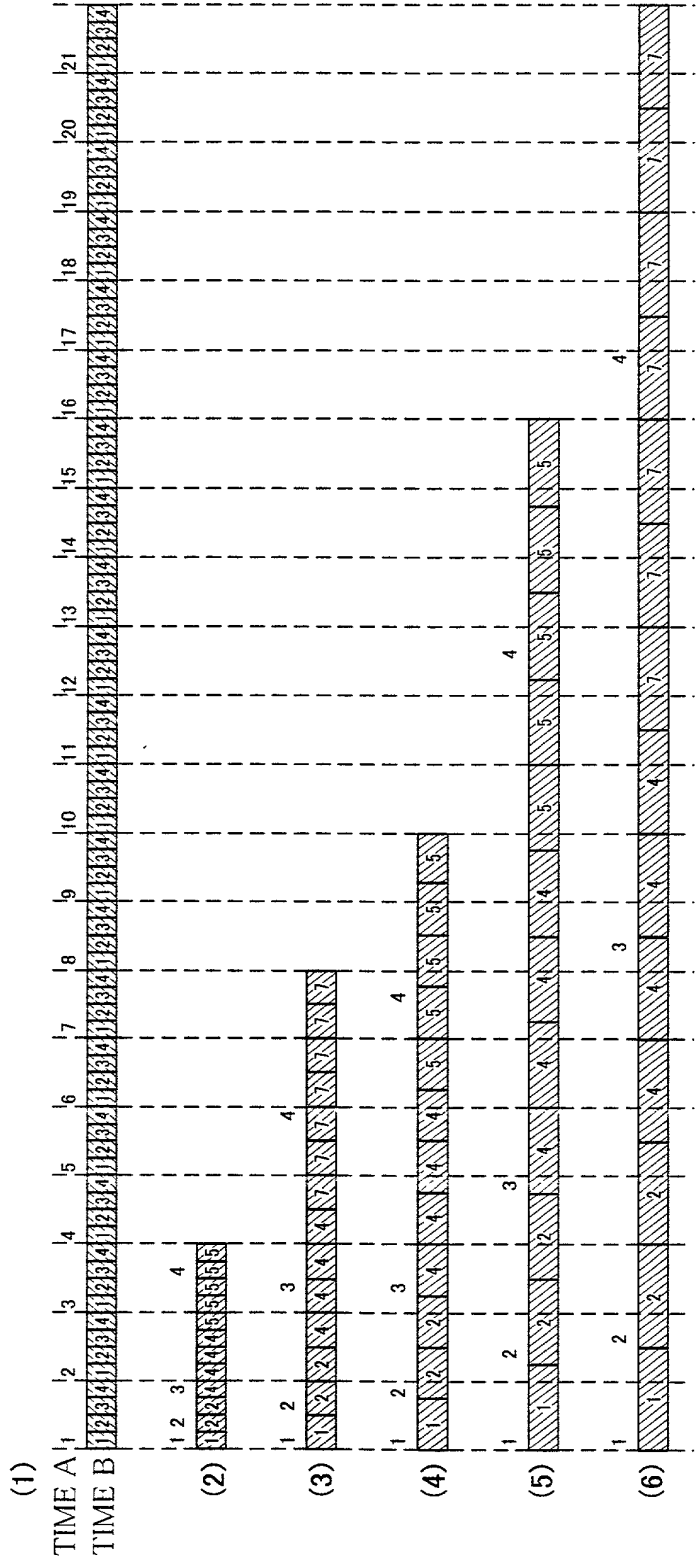


Figure 1 is a Gantt chart illustrating the scheduling of 21 tasks (T1 to T21) on a single processor. The chart shows the execution timeline for each task, with tasks T1 through T10 having deadlines. Tasks are represented by horizontal bars, some with diagonal hatching. Task T1 is a long bar at the top. Tasks T2 through T10 are shorter bars below it, with varying start and end times. Task T11 is a long bar at the bottom. The x-axis is labeled 'TIME' and has markers for each task's duration.

FIG. 25

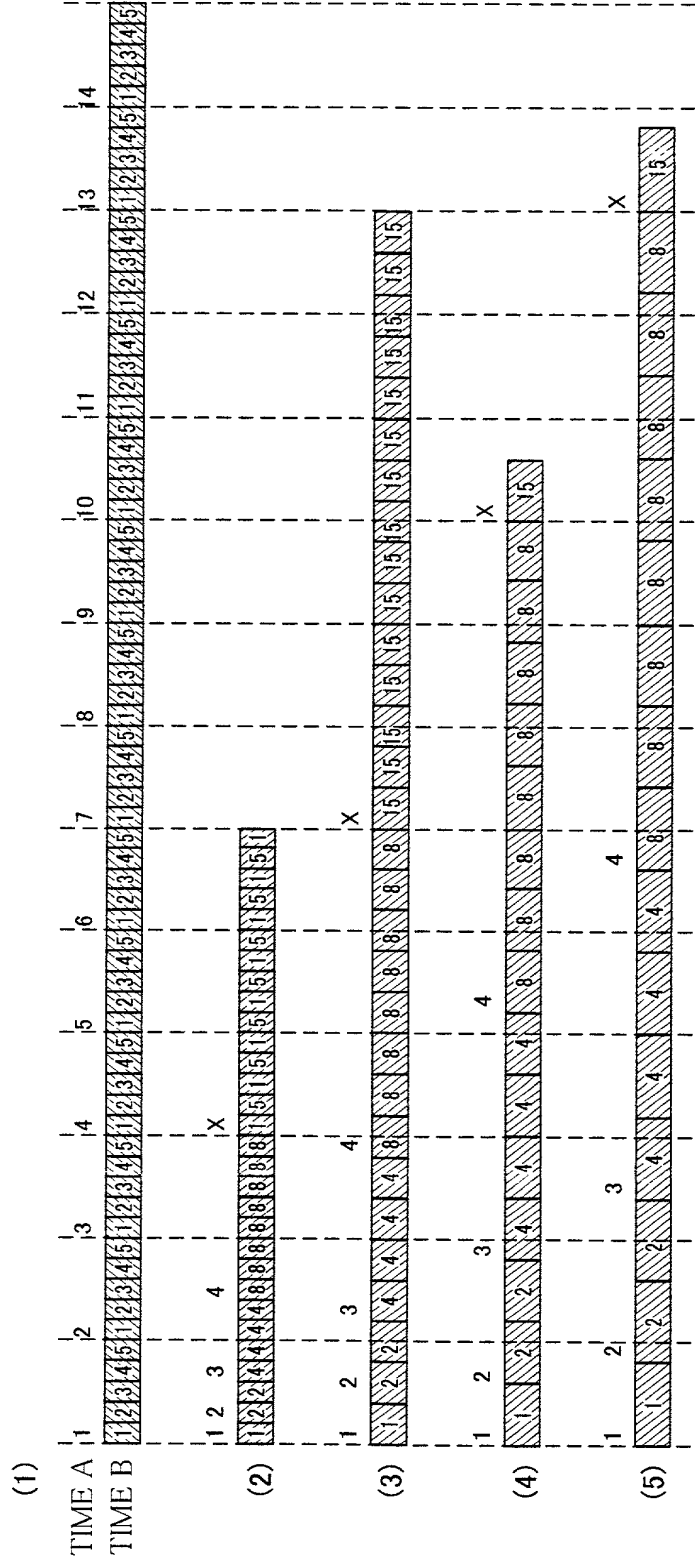


FIG. 26

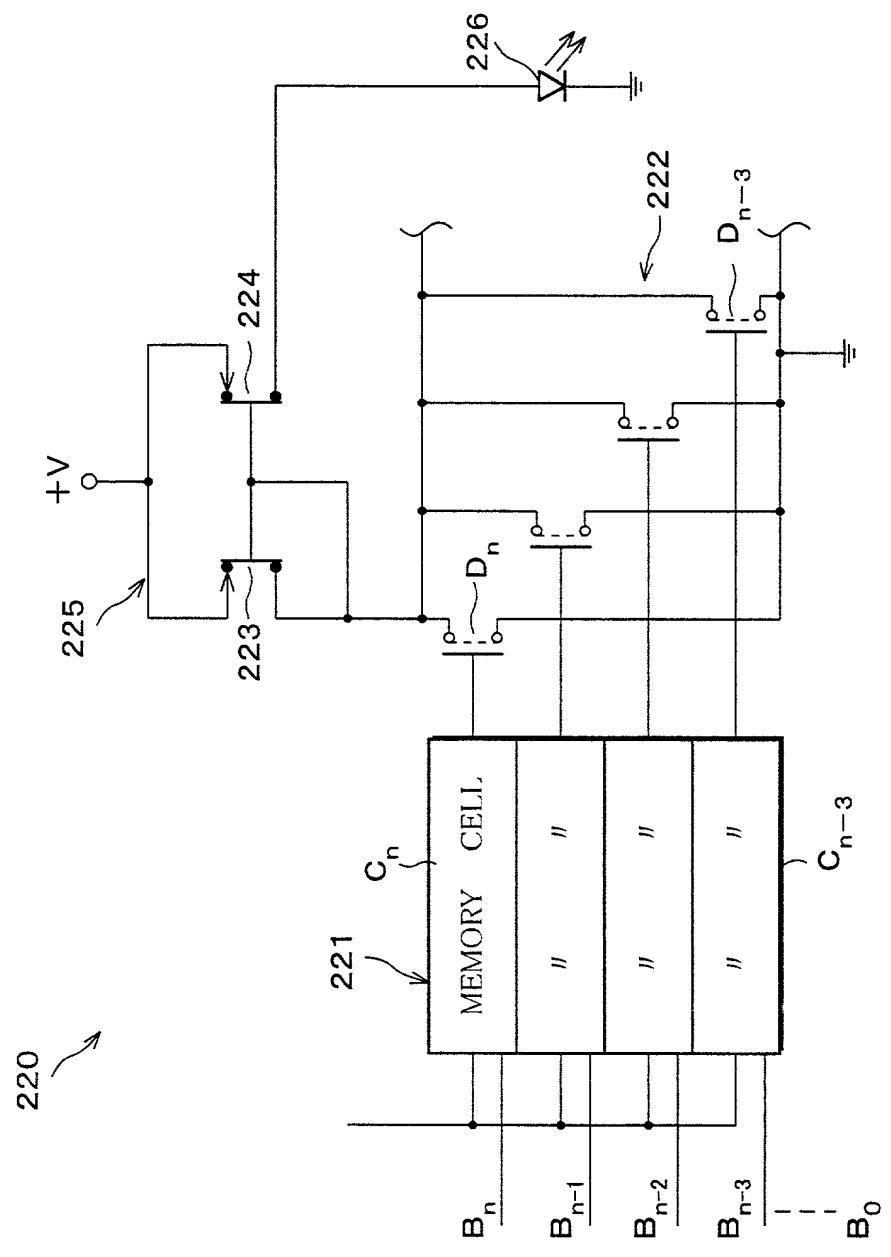


FIG. 27

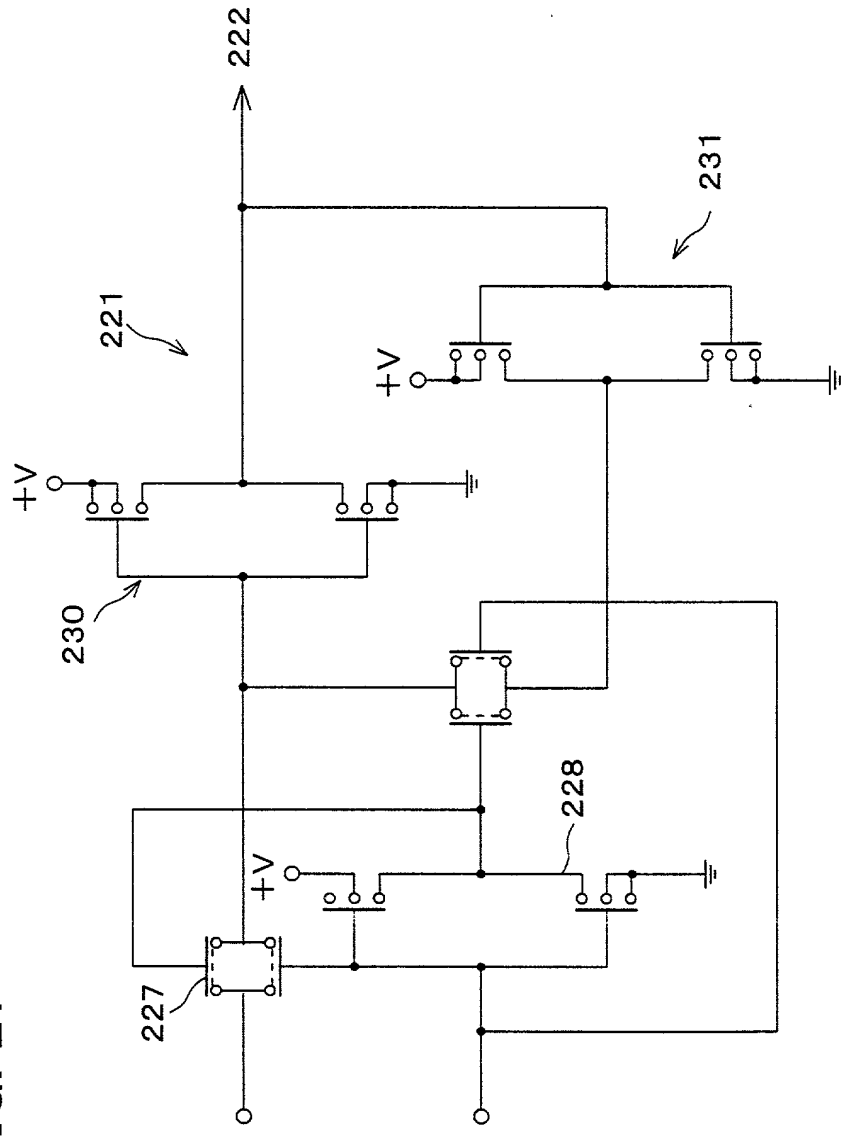
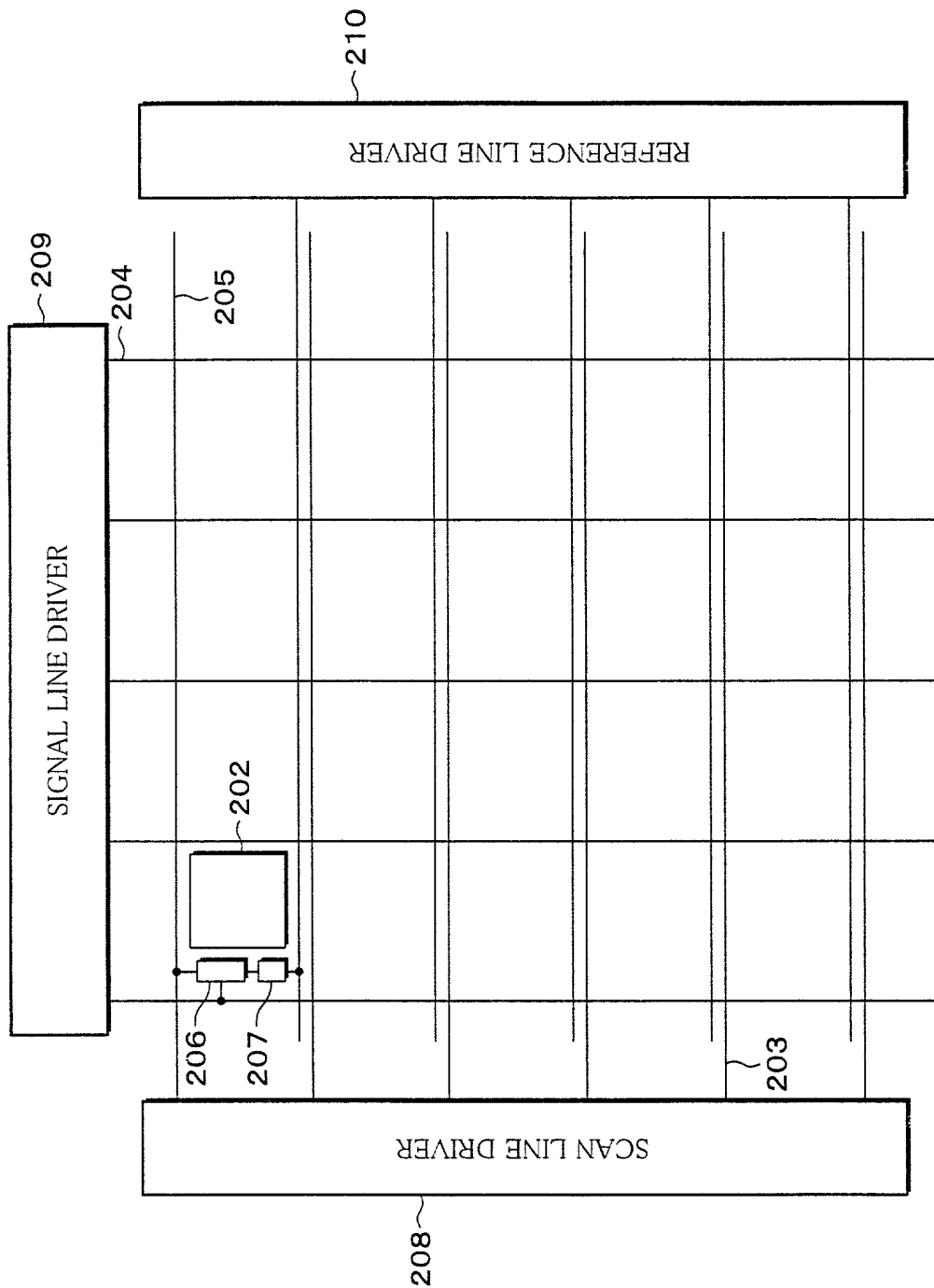


FIG. 28



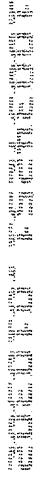
[illegible]

FIG. 30

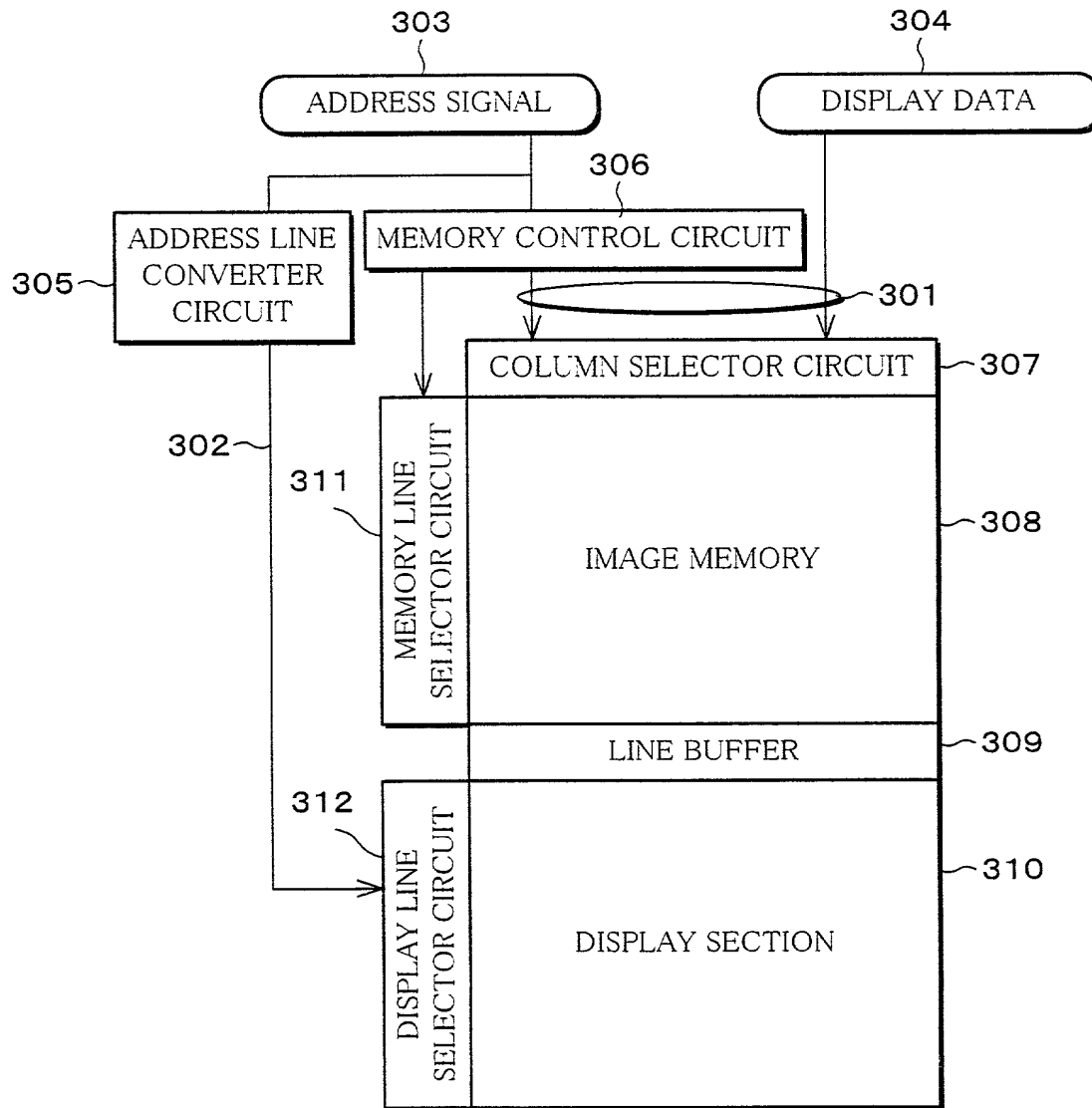


FIG. 31

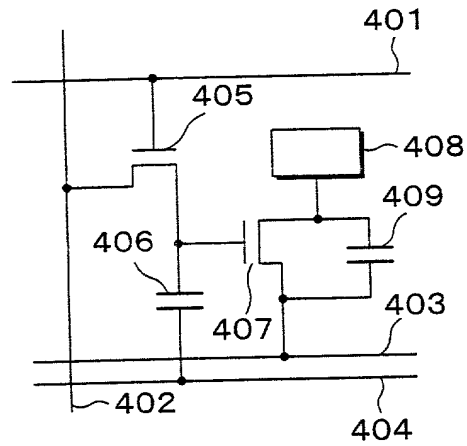


FIG. 32

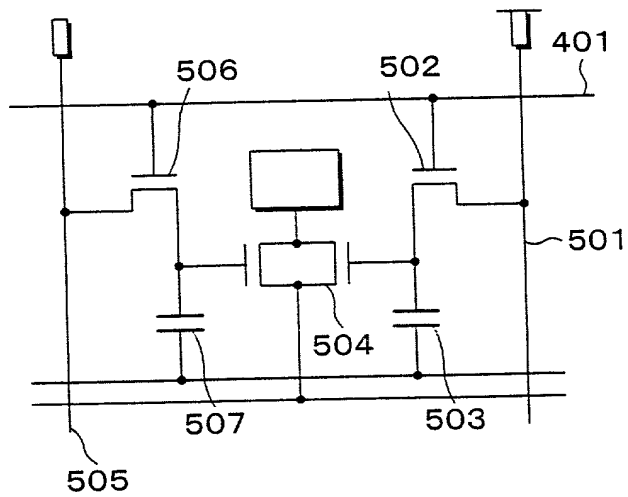


FIG. 33

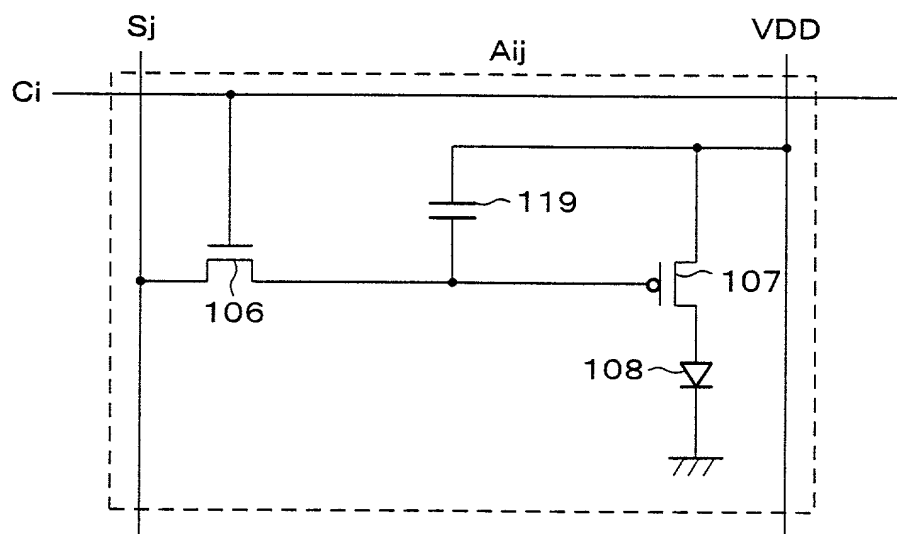
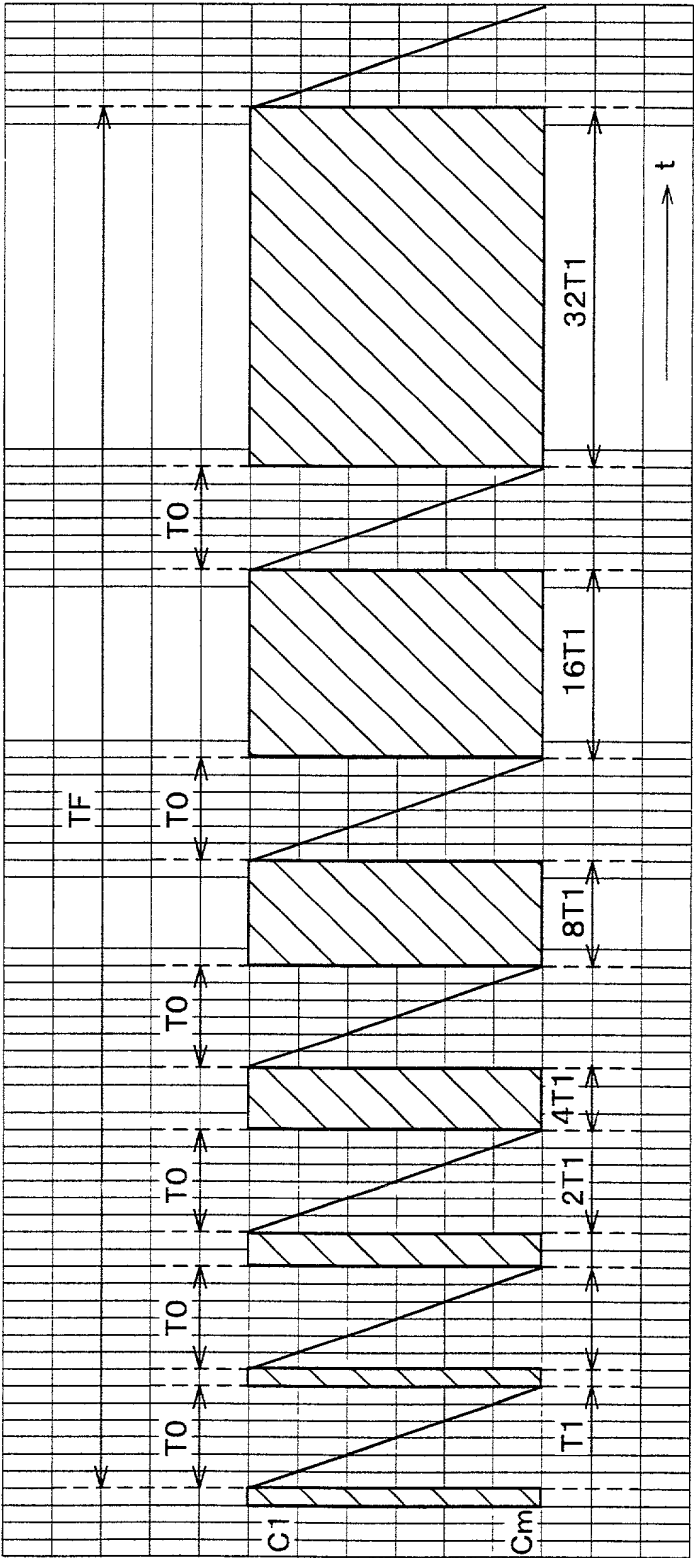


FIG. 34



The diagram illustrates the cross-sectional evolution of a material through various stages. It shows multiple layers labeled C1, Cm, (31), (32), and (33). Key dimensions along the vertical axis include T0, TF, T1, 2T1, 4T1, 8T1, 16T1, and 32T1. Arrows indicate the direction of flow or movement.